Document Number: MC33660
Rev 3.0, 10/2011

RoHS

ISO K Line Serial Link Interface

33660

ISO9141 PHYSICAL INTERFACE

EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

The 33660 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller, and systems off-board the vehicle via the special ISO K line. The 33660 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and over-temperature conditions.

The 33660 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the 33660 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of -40 ºC ≤ T_A ≤ 125 ºC and 8.0 V ≤ V_{BB} ≤ 18 V supply. The economical SO-8 surface-mount plastic package makes the 33660 very cost effective.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33660EF/R2	-40 to 125 °C	8-SOICN

Features

- Operates over wide supply voltage of 8.0 to 18 V
- Operating temperature of -40 to 125 °C
- Interfaces directly to standard CMOS microprocessors
- ISO K line pin protected against shorts to battery
- Thermal shutdown with hysteresis
- ISO K line pin capable of high currents
- ISO K line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components
- Standby mode: no V_{BAT} current drain with V_{DD} at 5.0 V
- Low current drain during operation with V_{DD} at 5.0 V

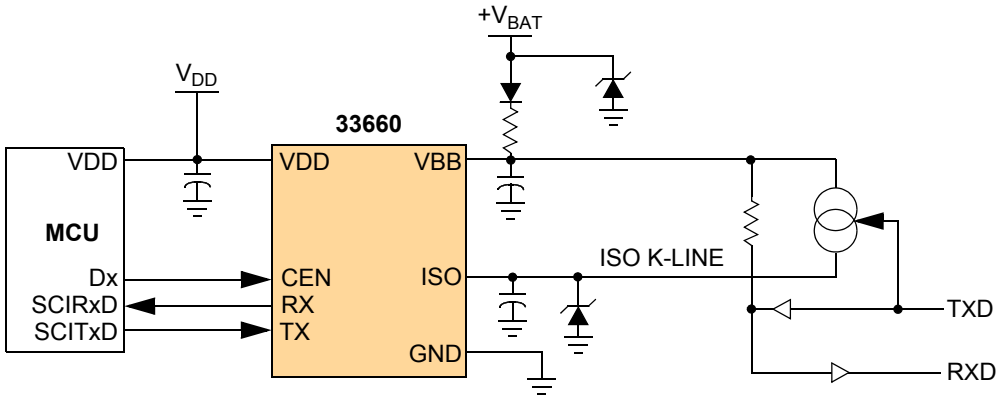

Figure 1. 33660 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

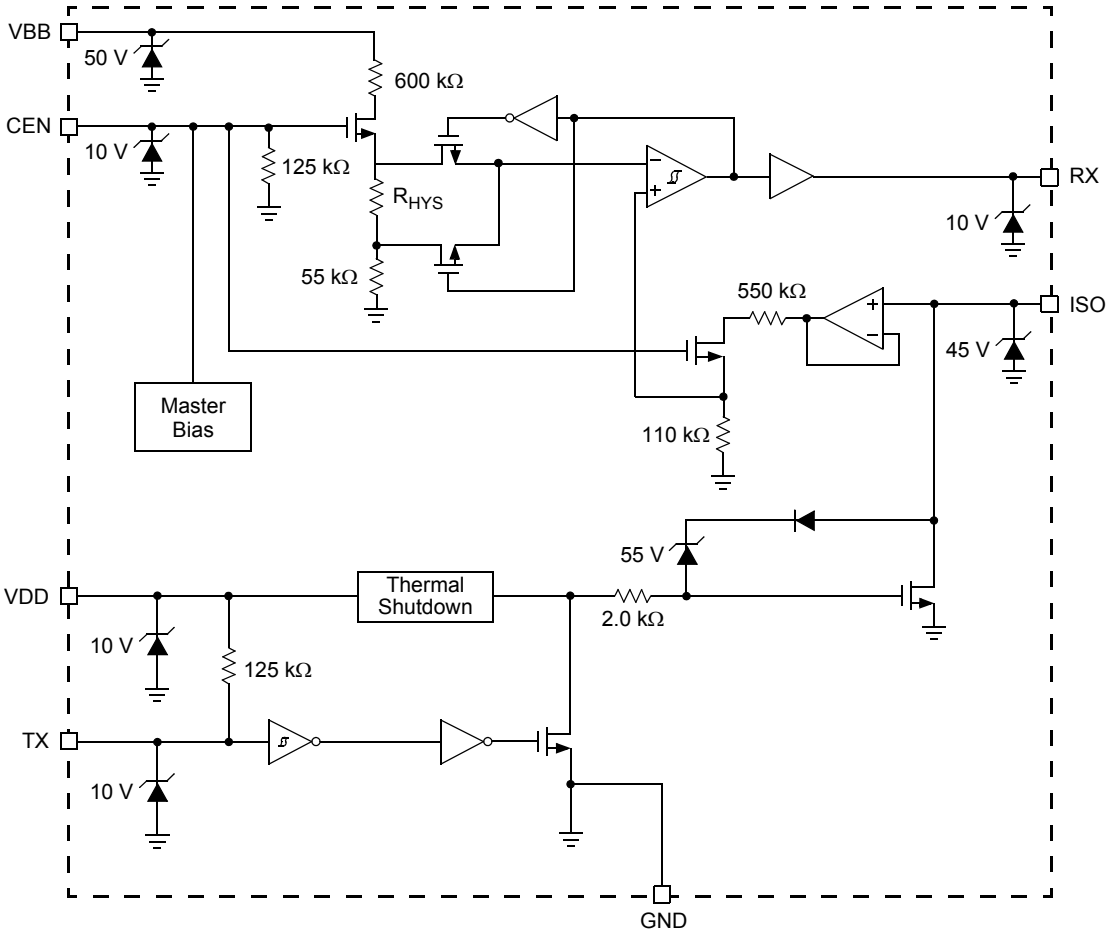


Figure 2. 33660 Simplified Internal Block Diagram

PIN CONNECTIONS

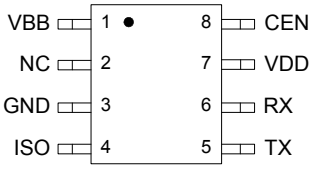


Figure 3. 33660 Pin Connections

Table 1. 33660 Pin Definitions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. (1)
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic “1” for active state. Logic “0” for sleep state.

Notes

1. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
VDD DC Supply Voltage	V_{DD}	-0.3 to 7.0	V
VBB Load Dump Peak Voltage	$V_{BB(LD)}$	45	V
ISO Pin Load Dump Peak Voltage (2)	V_{ISO}	40	V
ESD Voltage (3)			V
Human Body Model (4)	V_{ESD1}	±2000	
Machine Model (4)	V_{ESD2}	±200	
Charge Device Model (4)			
Corner Pins	V_{ESD3-1}	±750	
All other Pins	V_{ESD3-2}	±500	
ISO Clamp Energy (5)	E_{CLAMP}	10	mJ
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Case Temperature	T_C	-40 to +125	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Power Dissipation T_A = 25 °C	P_D	100	mW
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7.	°C
Thermal Resistance: Junction-to-Ambient	$R_{\theta JA}$	150	°C/W

Notes

2. Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
3. ESD data available upon request.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), ESD3 testing is performed in accordance with the Charge Device Model (C_{ZAP} = 4.0 pF).
5. Nonrepetitive clamping capability at 25 °C.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V_{DD} Sleep State Current T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{DD(SS)}$	–	–	0.1	mA
V_{DD} Quiescent Operating Current T_x = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{DD(Q)}$	–	–	1.0	mA
V_{BB} Sleep State Current V_{BB} = 16 V, T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{BB(SS)}$	–	–	50	µA
V_{BB} Quiescent Operating Current T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High Voltage Threshold [8] Input Low Voltage Threshold [9]	 $V_{IH(CEN)}$ $V_{IL(CEN)}$	 0.7 V_{DD} –	 – –	 – 0.3 V_{DD}	V
Chip Enable Pull-down Current [10]	$I_{PD(CEN)}$	2.0	–	40	µA
T_X Input Low Voltage Threshold R_{ISO} = 510 Ω [11]	$V_{IL(TX)}$	–	–	0.3 x V_{DD}	V
T_X Input High Voltage Threshold R_{ISO} = 510 Ω [12]	$V_{IH(TX)}$	0.7 x V_{DD}	–	–	V
T_X Pull-up Current [13]	$I_{PU(TX)}$	-40	–	-2.0	µA
R_X Output Low Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}, R_x Sinking 1.0 mA	$V_{OL(RX)}$	–	–	0.2 V_{DD}	V
R_X Output High Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}, R_X Sourcing 250 µA	$V_{OH(RX)}$	0.8 V_{DD}	–	–	V
Thermal Shutdown [14]	T_{LIM}	150	170	–	°C

Notes

8. When I_{BB} transitions to >100 µA.
9. When I_{BB} transitions to <100 µA.
10. Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at 0.3 V_{DD}.
11. Measured by ramping T_X down from 0.8 V_{DD} and noting T_X value at which ISO falls below 0.2 V_{BB}.
12. Measured by ramping T_X up from 0.2 V_{DD} and noting the value at which ISO rises above 0.9 V_{BB}.
13. T_x pin has internal current pull-up. Pull-up current is measured with T_X pin at 0.7 V_{DD}.
14. Thermal Shutdown performance (T_{LIM}) is guaranteed by design, but not production tested.

Table 3. Static Electrical Characteristics (Continued)

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
Input Low Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}	$V_{IL(ISO)}$	–	–	0.4 x V_{BB}	V
Input High Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}	$V_{IH(ISO)}$	0.7 x V_{BB}	–	–	V
Input Voltage Hysteresis	$V_{HYS(ISO)}$	0.05 x V_{BB}	–	0.1 x V_{BB}	V
Internal Pull-up Current R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}, V_{ISO} = 9.0 V, V_{BB} = 18 V	$I_{PU(ISO)}$	-5.0	–	-140	µA
Short-circuit Current Limit R_{ISO} = 0 Ω, T_X = 0.4 V_{DD}, V_{ISO} = V_{BB}	$I_{SC(ISO)}$	50	–	200	mA
Output Low Voltage R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}	$V_{OL(ISO)}$	–	–	0.1 x V_{BB}	V
Output High Voltage R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}	$V_{OH(ISO)}$	0.95 x V_{BB}	–	–	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time (15) R_{ISO} = 510 Ω to V_{BB}, C_{ISO} = 10 nF to Ground	$t_{FALL(ISO)}$	–	–	2.0	µs
ISO Propagation Delay (16) High to Low: R_{ISO} = 510 Ω, C_{ISO} = 500 pF (17) Low to High: R_{ISO} = 510 Ω, C_{ISO} = 500 pF (18)	$t_{PD(ISO)}$	– –	– –	2.0 2.0	µs

Notes

15. Time required ISO voltage to transition from 0.8 V_{BB} to 0.2 V_{BB}.
16. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
17. Step T_X voltage from 0.8 V_{DD} to 0.2 V_{DD}. Time measured from $V_{IH(Tx)}$ until V_{ISO} reaches 0.3 V_{BB}.
18. Step T_X voltage from 0.2 V_{DD} to 0.8 V_{DD}. Time measured from $V_{IL(Tx)}$ until V_{ISO} reaches 0.7 V_{BB}.

ELECTRICAL PERFORMANCE CURVES

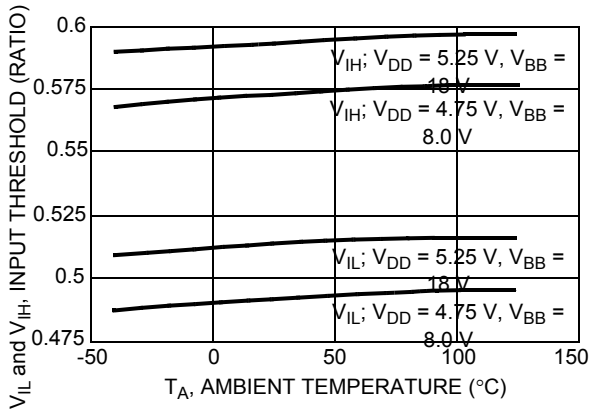


Figure 4. ISO Input Threshold/V_{BB} vs. Temperature

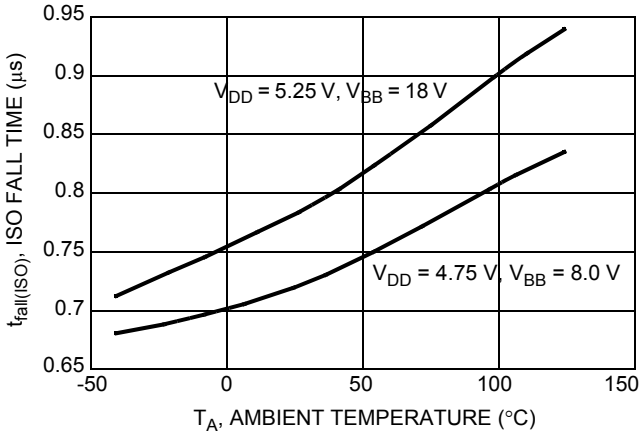


Figure 5. ISO Output/V_{BB} vs. Temperature

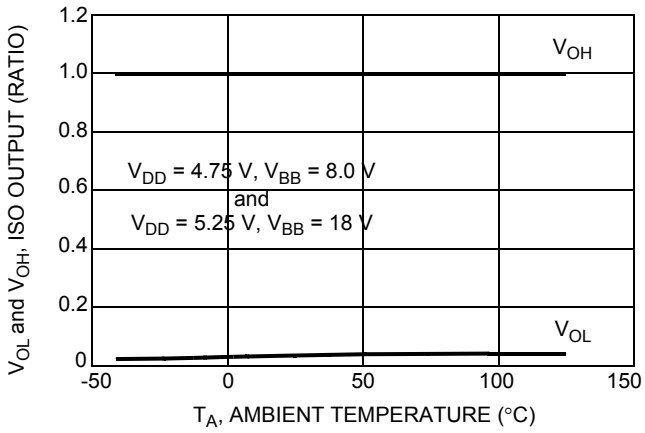


Figure 6. ISO Fall Time vs. Temperature

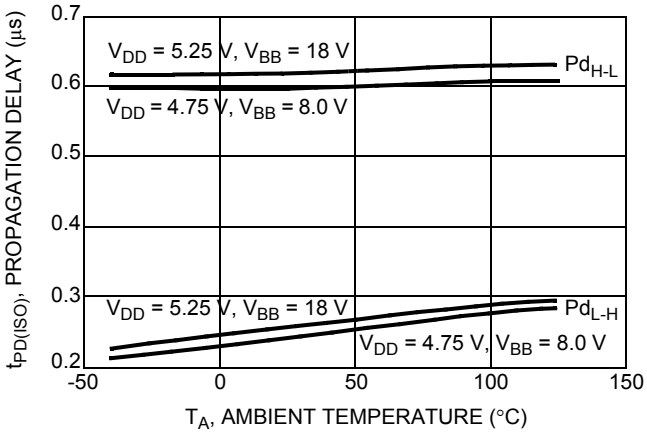


Figure 7. ISO Propagation Delay vs. Temperature

TYPICAL APPLICATIONS

INTRODUCTION

The 33660 is a serial link bus interface device conforming to the ISO 9141 physical bus specification. The device is designed for automotive environment usage, compliant with On-board Diagnostics (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line. The device does not incorporate an ISO L line. It provides bi-directional half-duplex communications interfacing from a microcontroller to the communication bus. The 33660 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic, and from battery level logic to 5.0 V logic levels. The 33660 is built using Freescale Semiconductor's SMARTMOS process and is packaged in an 8-pin plastic SOIC.

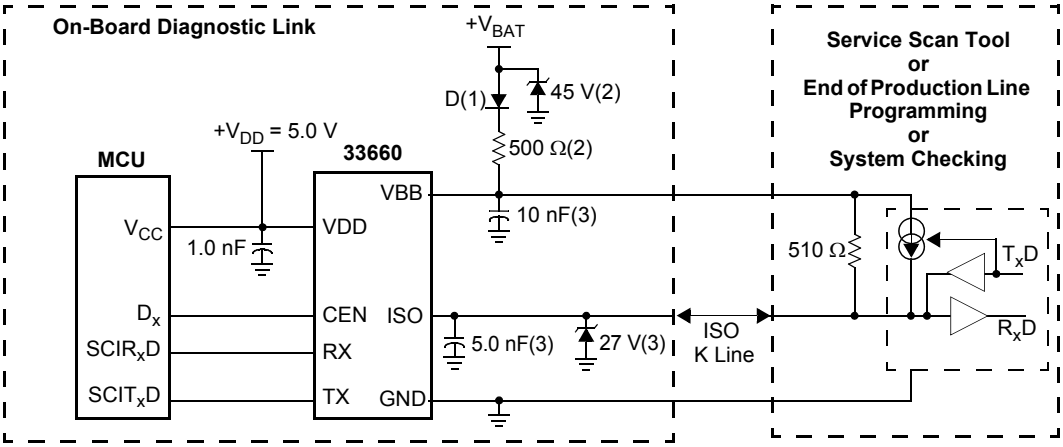
FUNCTIONAL DESCRIPTION

The 33660 transforms 5.0 V microcontroller logic signals to battery level logic signals and visa versa. The maximum data rate is set by the rise and fall time. The fall time is set by the output driver. The rise time is set by the bus capacitance and the pull-up resistors on the bus. The fall time of the 33660 allows data rates up to 150 kbps using a 30 percent maximum bit time transition value. The serial link interface will remain fully functional over a battery voltage range of 6.0 to 18 V. The device is parametrically specified over a dynamic V_{BB} voltage range of 8.0 to 18 V.

Required input levels from the microcontroller are ratio-metric with the V_{DD} voltage normally used to power the microcontroller. This enhances the 33660's ability to remain in harmony with the R_X and T_X control input signals of the microcontroller. The R_X and T_X control inputs are compatible with standard 5.0 V CMOS circuitry. For fault tolerant purposes the T_X input from the microcontroller has an internal passive pull-up to V_{DD}, while the CEN input has an internal passive pull-down to ground.

A pull-up to battery is internally provided as well as an active data pull-down. The internal active pull-down is current-limit protected against shorts to battery, and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external 510 Ω pull-up resistor and a diode to battery.

Reverse battery protection of the device is provided by the use of a reverse battery blocking diode (See "D" in the Typical Application Diagram on page 9). Battery line transient protection of the device is provided for by using a 45 V zener and a 500 Ω resistor connected to the V_{BB} source, as shown in the same diagram. Device ESD protection from the communication lines exiting the module is through the use of the capacitor connected to the V_{BB} device pin, and the capacitor used in conjunction with the 27 V zener connected to the ISO pin.



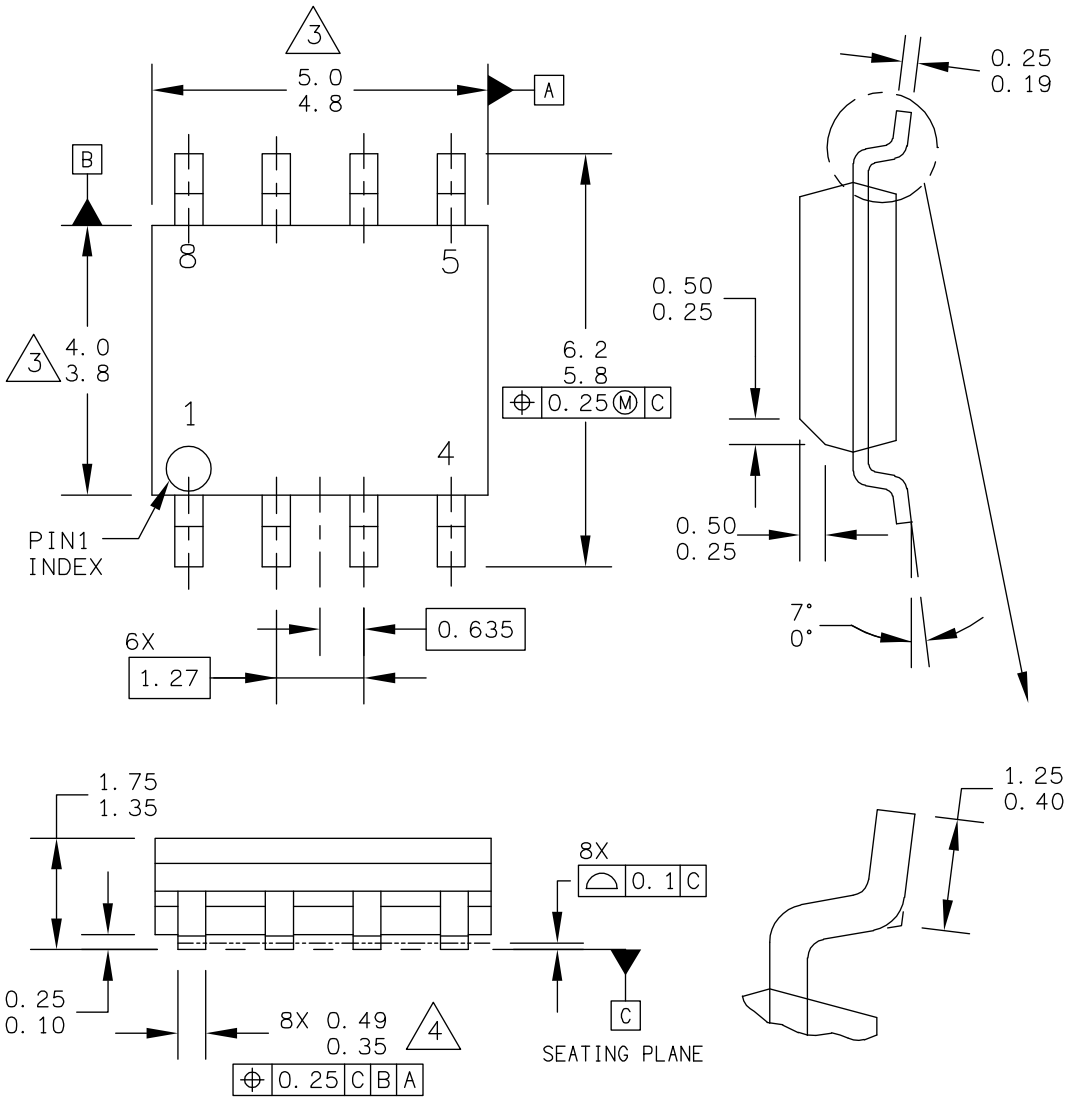
Components necessary for Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case.

Figure 8. Typical Application Diagram

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)
8-PIN
98ASB42564B
REV. V

33660

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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8LD SOIC NARROW BODY	CASE NUMBER: 751–07	20 NOV 2007
	STANDARD: JEDEC MS–012AA	

EF SUFFIX (PB-FREE)
8-PIN
98ASB42564B
REV. V

33660

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	1/2011	• Initial release
2.0	9/2011	• Adjusted format to meet current compliance standards. No data was altered.
3.0	10/2011	• Updated the PC part number to MC.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
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